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What is claimed is:

1 1. A method of making a multiple gate electrode on a semiconductor device, comprising the  
2 steps of:

3 coating a layer of gate electrode material over a semiconductor device that has been  
4 previously coated with a thin film of gate dielectric; and

5 planarizing the layer of gate electrode material to a substantially planar surface prior to  
6 patterning the gate electrode material to form a discrete multiple gate electrode on the  
7 semiconductor device.

1 2. The method of claim 1, further comprising the steps of:

2 applying a photoresist mask of substantially uniform thickness on the planar top surface  
3 of the planarized gate electrode material;

4 patterning the photoresist mask to cover a corresponding pattern of the discrete multiple  
5 gate electrode; and

6 etching the gate electrode material that is uncovered by the photoresist mask to form the  
7 discrete multiple gate electrode.

1 3. The method of Claim 1, further comprising the step of:

2 conforming the layer of gate electrode material with a step height increase corresponding  
3 to an increased step height of the semiconductor device.

4 4. The method of claim 1 wherein, the semiconductor device comprises a silicon fin.

5 5. The method of claim 1 wherein, the semiconductor device comprises a fin of silicon and  
2 germanium.

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- 6  
1 ~~6~~. The method of claim 1, further comprising the steps of:
- 2       applying a photoresist mask of substantially uniform thickness on the planar top surface  
3 of the planarized gate electrode material, the mask comprising photoresist and a mask material  
4 selected from the group comprising, silicon nitride, silicon oxynitride, silicon oxide and photo  
5 resist, or combinations thereof;
- 6       patterning the photoresist mask to cover a corresponding pattern of the multiple gate  
7 electrode; and
- 8       etching the gate electrode material that is uncovered by the photoresist mask to form the  
9 discrete multiple gate electrode.

- 7  
1 ~~7~~. The method of claim 1, further comprising the steps of:
- 2       applying a photoresist mask of substantially uniform thickness on the planar top surface  
3 of the planarized gate electrode material;
- 4       patterning the photoresist mask to cover a corresponding pattern of the multiple gate  
5 electrode; and
- 6       plasma etching the gate electrode material that is uncovered by the photoresist mask to  
7 form the patterned multiple gate electrode.

- 8  
1 ~~8~~. The method as recited in claim 1, further comprising the step of: applying a mask over  
2 the planarized surface, wherein the mask is of substantially uniform thickness for accurate  
3 patterning thereof.

- 9  
1 ~~9~~. The method of claim 1 wherein, the gate dielectric comprises silicon oxide.

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1 ~~9.~~ The method of claim 1 wherein, the gate dielectric comprises silicon oxynitride.
- 11  
1 ~~10.~~ The method of claim 1 wherein, the gate dielectric comprises a high permittivity material.
- 12  
1 ~~11.~~ The method of claim 1 wherein, the gate dielectric comprises a material having a  
2 permittivity greater than 5.
- 13  
1 ~~12.~~ The method of claim 1 wherein, the gate dielectric comprises a thickness in the range of 3  
2 and 100 Angstroms.
- 14  
1 ~~13.~~ The method of claim 1 wherein, the multiple gate electrode comprises polycrystalline  
2 silicon.
- 15  
1 ~~14.~~ The method of claim 1 wherein, the multiple gate electrode comprises a conductive  
2 material.
- 16  
1 ~~15.~~ The method of claim 1 wherein, the multiple gate electrode comprises a metal material.
- 17  
1 ~~16.~~ A semiconductor device having a multiple gate electrode, comprising:  
2 the semiconductor device having a projecting fin;  
3 a multiple gate electrode on more than one side of the fin, the multiple gate electrode  
4 having a substantially planar surface extending over the fin; and  
5 a patterned mask on the planar surface of the multiple gate electrode, the patterned mask  
6 having a substantially uniform thickness and a substantially planar surface.
- 18  
1 ~~17.~~ The semiconductor device of claim <sup>17</sup>~~16~~ wherein, the multiple gate electrode is a portion of  
2 a layer of gate electrode material having a planarized surface, and the planarized surface includes  
3 the planar surface of the multiple gate electrode.